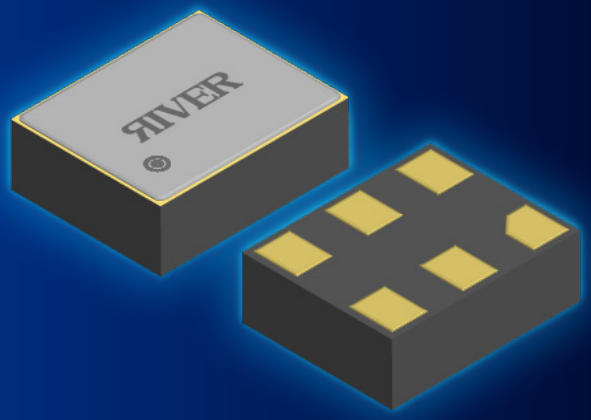
What Should Be Evaluated for 1.6T Optical Communications Clocks? Key Points for Confirming Clock Quality and Reducing Design Risk

KCRO-05

Ultra-Low-Jitter Crystal Oscillator for AI Data Centers

- 625 MHz PLL-Free Direct Oscillation
- Typ. 12 fs RMS Phase Jitter
- 12 kHz–20 MHz



White Paper

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Introduction

In 1.6T optical communications, as transmission speeds increase, even slight phase fluctuations contained in the clock can reduce timing margin and potentially affect BER (bit error rate) and system stability. When evaluating a clock, catalog jitter values alone are not sufficient; it is important to confirm suitability for your own boards and operating environment.

Technical materials submitted to the IEEE P802.3dj Task Force also indicate that small phase errors can affect BER in high-speed communications. To minimize rework in the later stages of design, phase noise, RMS phase jitter, temperature characteristics, implementation conditions, and other factors should be organized from the early design stage, and evaluation conditions should be clearly defined.

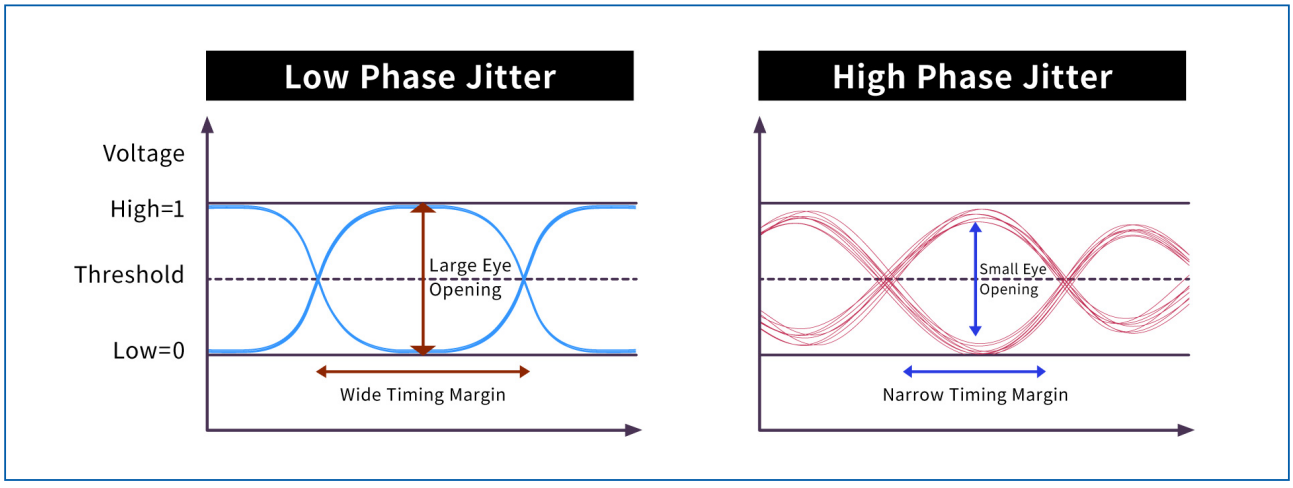
This document organizes the evaluation criteria to consider when selecting clocks for 1.6T optical communications, explains how to interpret catalog specifications and general evaluation data, and describes the points to confirm before proceeding with evaluation in your own environment.

Why Evaluating Clock Quality Is Critical in 1.6T Optical Communication

In 1.6T optical communication, increasing transmission speeds make the overall system more susceptible to even slight phase fluctuations and timing variations originating from the clock. It is therefore important to evaluate not only the standalone performance of the clock, but also its impact on timing margin and bit error rate (BER), as well as the risk of costly design rework during the later stages of development.
This section examines why clock quality evaluation has become such an important consideration in high-speed communication system design.

Higher Speeds Make It More Difficult to Maintain Sufficient Timing Margin

In 1.6T optical communication, maintaining sufficient timing margin becomes increasingly important as transmission speeds rise. With next-generation high-speed lanes such as 224G SerDes, the time available for each symbol becomes shorter, making receiver timing more susceptible to even slight phase fluctuations in the clock.
Technical materials submitted to the IEEE P802.3dj Task Force have also indicated that small phase errors can affect bit error rate (BER) in bandwidth-limited high-speed communication systems. Designers must therefore consider the overall jitter budget, including not only the clock but also PLLs, drivers, power-supply noise, and PCB transmission paths.
In addition to the integration bandwidth and measurement conditions used for RMS phase jitter, designers should also confirm the difference between Typ. and Max. values and evaluate clock performance under conditions that reflect the requirements of their own system design.



Clock Quality Affects Receiver Timing Margin and Bit Error Rates

Clock quality is an important factor in determining the margin available for the receiver to correctly detect signals. As phase jitter increases, variations in signal decision timing can become greater, potentially affecting bit error rate (BER) and FEC performance.
Technical materials submitted to the IEEE P802.3dj Task Force have also indicated that uncorrelated jitter can broaden the phase distribution and potentially affect the quality of high-speed communication. However, the jitter metrics used for transmitted signals in these materials and the RMS phase jitter of an oscillator differ in both what is measured and how the measurements are performed. Their numerical values therefore cannot be directly compared.
When evaluating a clock, it is important to confirm factors such as the integration bandwidth, measurement conditions, output format, and termination conditions, and comprehensively determine whether the clock performance is consistent with the overall system jitter budget.

Defining Evaluation Conditions Early Helps Minimize Design Rework

In 1.6T optical communication, multiple factors can affect clock quality, including heat generated by high-density integration, power-supply noise, PCB configuration, and interference from surrounding circuitry. It is therefore important to define the relevant evaluation criteria from the candidate selection stage, taking into account the operating conditions expected in the actual system.
If BER degradation or unstable synchronization is discovered during the later stages of development, it can result in PCB redesign, repeated evaluation, and even revisions to the mass-production schedule. From the early stages of system design, designers should therefore establish requirements for factors such as jitter, frequency accuracy, and temperature characteristics, clearly define evaluation conditions including the operating temperature range and power-supply conditions, and compare candidate devices accordingly.
Establishing an evaluation plan with sufficient design margin early in the development process makes it easier to isolate potential issues during later stages and helps minimize costly design rework.

Three Key Evaluation Criteria for Selecting Clocks for 1.6T Optical Communication

When evaluating a clock, the decision cannot be based on a single specification alone. In 1.6T optical communication, it is important to evaluate not only the quality of the clock signal itself, but also performance under the intended operating environment and mounting conditions.
This section outlines three key evaluation criteria to consider when comparing and selecting candidate clock devices.

Three Key Evaluation Criteria for Selecting Clocks for 1.6T Optical Communication

Evaluate overall compatibility with the actual system, not a single specification.

01

Phase Noise / RMS Phase Jitter

- Phase Noise
- RMS Phase Jitter
- Integration Bandwidth
- Measurement Conditions

Does it meet the required timing performance?

02

Frequency-Temperature Characteristics

- Frequency Variation
- Operating Temperature Range
- High-Temperature Conditions
- Measurement Conditions

Is it stable across the expected temperature range?

03

Compatibility with Specifications and Operating Conditions

- Frequency / Output Format
- Termination / Supply Voltage
- Package Size
- Recommended Mounting Conditions

Is it compatible with the board design?

Confirm compatibility with the actual system requirements and operating conditions.

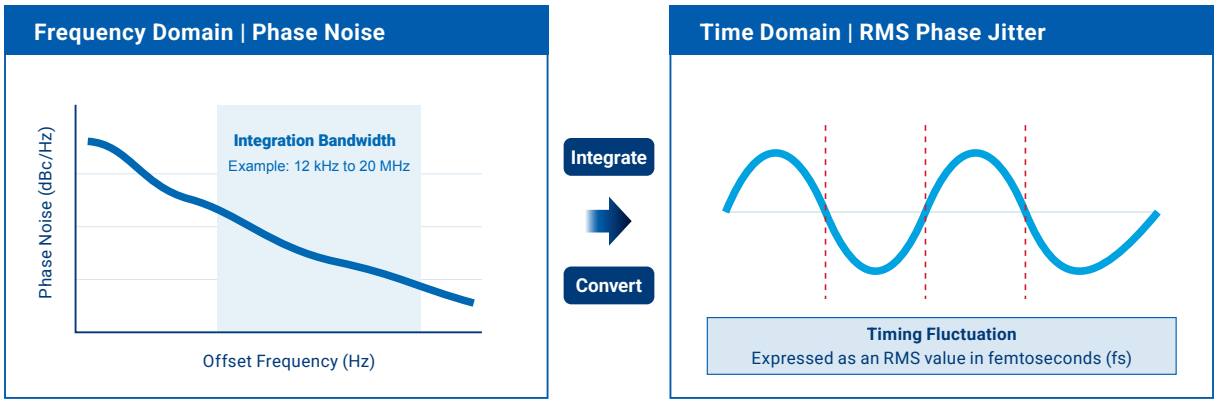
Use the three criteria together when narrowing down candidates for evaluation.

Phase Noise / RMS Phase Jitter

Phase noise and RMS phase jitter are among the first metrics to consider when evaluating clock quality for 1.6T optical communication. It is important to understand what each metric represents and to compare performance while also taking the measurement conditions into account.

Relationship Between Phase Noise and RMS Phase Jitter

The same phase fluctuation is evaluated from different perspectives.



CAUTION **Do not directly compare data measured under different integration bandwidths, oscillation frequencies, supply conditions, or load conditions.**

Conceptual diagram. The phase-noise curve is not measured data for a specific product.

① What Does It Measure?

Phase noise is a metric that represents phase fluctuations in a clock signal in the frequency domain. RMS phase jitter quantifies phase noise over a specified integration bandwidth as timing fluctuations in the time domain. In other words, the two metrics evaluate the same phase fluctuations from different perspectives.

② Why Is It Important in 1.6T Optical Communication Design?

In 1.6T optical communication, increasing transmission speeds mean that even slight phase fluctuations can potentially affect timing margin and bit error rate (BER). In IEEE P802.3dj, metrics such as J3u/J6u, in addition to JRMS, are being considered during the standardization process to evaluate transmitted signals, including the tails of the jitter distribution. These discussions highlight the importance of evaluating not only the magnitude of jitter but also its distribution in high-speed communication.
However, these transmitted-signal jitter metrics and the RMS phase jitter of an oscillator differ in both what they measure and how they are measured. Their numerical values should therefore not be directly compared.

③ What Should Be Checked When Comparing and Evaluating Clocks?

In addition to the RMS phase jitter value itself, designers should confirm the integration bandwidth, oscillation frequency, phase noise plot, power-supply conditions, load conditions, and other measurement conditions. Rather than looking only at jitter values obtained over a specified integration bandwidth, such as 12 kHz to 20 MHz, it is important to examine phase noise over a broader frequency range, as well as frequency bands to which the actual circuit may be particularly sensitive.
Data obtained under different measurement conditions should not be compared at face value. Instead, clock performance should be evaluated against the requirements and operating conditions of the actual system design.
Phase noise and RMS phase jitter provide important information when establishing the overall system jitter budget. Designers should therefore evaluate not only the numerical values themselves, but also the measurement conditions under which those values were obtained.

Frequency-Temperature Characteristics

Frequency-temperature characteristics are an important evaluation criterion for determining whether a clock can maintain stable operation under actual operating conditions. In 1.6T optical communication equipment, particularly in high-temperature environments, the ability to maintain stable frequency performance across temperature variations becomes especially important.

① What Does It Measure?

Frequency-temperature characteristics indicate how the oscillation frequency changes in response to temperature variations. In addition to frequency accuracy at a specific temperature, designers should examine the amount of frequency variation across the entire intended operating temperature range, as well as whether the frequency changes smoothly with temperature.

② Why Is It Important in 1.6T Optical Communication Design?

In optical transceivers and AI data center equipment, heat generated by high-density integration can expose clocks to high-temperature environments. Maintaining stable frequency characteristics across the intended operating conditions, including at higher temperatures, is therefore important for ensuring reliable communication quality.

③ What Should Be Checked When Comparing and Evaluating Clocks?

Designers should confirm not only the amount of frequency variation, but also the temperature range and measurement conditions used for evaluation. It is also important to verify that the specified range covers the actual operating temperature range of the system and that the frequency changes smoothly as the temperature varies. These factors make it easier to determine whether the clock is suitable for the intended operating environment.
Frequency-temperature characteristics should therefore be evaluated not only based on datasheet specifications, but also with the actual operating environment in mind.
Phase noise and RMS phase jitter provide important information when establishing the overall system jitter budget. Designers should therefore evaluate not only the numerical values themselves, but also the measurement conditions under which those values were obtained.

Compatibility with Specifications and Operating Conditions

To achieve the full performance of a clock device, designers must consider not only its specified performance values, but also its compatibility with the actual design requirements and mounting conditions of the system. When determining whether a clock is suitable for a particular application, it is essential to evaluate it from a system-level perspective that takes both the circuit design and PCB layout into account.

① What Does It Measure?

Key factors to confirm include the operating frequency, output format, termination conditions, supply voltage, operating temperature range, package size, and mounting conditions. Designers should also consider factors that can affect performance after mounting, including power-supply noise, power and GND design, and decoupling.

② Why Is It Important in 1.6T Optical Communication Design?

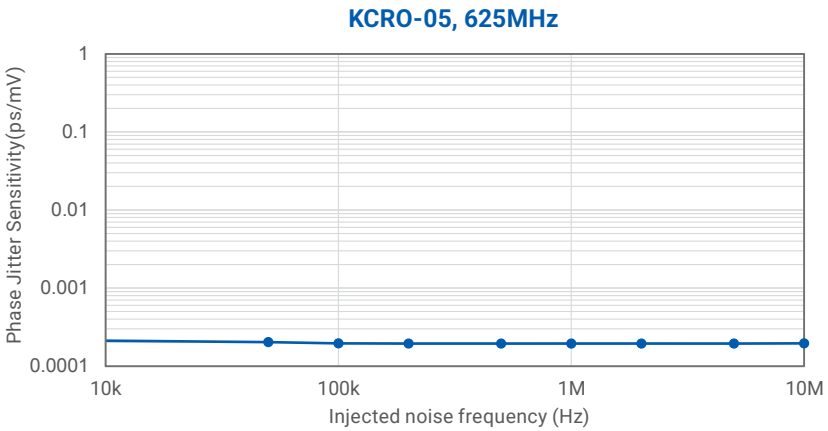
In equipment for 1.6T optical communication, high-density integration and high-speed signal transmission can increase susceptibility to power-supply noise, heat, and interference from surrounding circuitry. If the recommended termination circuit and mounting conditions are not properly implemented, the oscillator may not be able to deliver its full performance.

③ What Should Be Checked When Comparing and Evaluating Clocks?

Designers should confirm that the operating frequency, output format, supply voltage, and operating temperature range meet the system requirements. The termination conditions, recommended mounting conditions, and package size should also be checked against the PCB design. Where necessary, evaluating the clock under conditions that closely reflect the actual operating environment can help improve the accuracy of the final selection decision.
Confirming compatibility with the required specifications and operating conditions from the early stages of system design can help reduce the risk of costly design rework after evaluation or during mass production.

In addition, because clock performance can be affected by power supply noise, the sensitivity of phase jitter to power supply variations is another important parameter to evaluate. Reviewing the Phase Jitter Sensitivity data can help assess how changes in power supply conditions may affect phase jitter performance.

Phase Jitter Sensitivity



Why Datasheet Specifications and General Evaluation Data Alone Are Not Enough

Datasheet specifications and evaluation data provide important information for comparing candidate products, but they are not always sufficient to determine whether a clock is suitable for the actual operating environment of a particular system. Because the significance of measured values can vary depending on the measurement conditions and evaluation environment, it is important to confirm that the data is consistent with the system's own design requirements before proceeding with evaluation.
When reviewing evaluation data, designers should therefore consider not only the numerical values themselves, but also the conditions under which the data was obtained and differences in what was actually evaluated.

What Can Be Confirmed at Each Evaluation Stage

The closer the evaluation is to the actual system, the more directly compatibility can be confirmed.

》Closer to the Actual Operating Environment

01	02	02	02
Catalog Specifications	**Evaluation Board**	**Prototype Board**	**Mass Production / Actual Operating Environment**
■ Basic Specifications ■ Typical Performance ■ Measurement Conditions	■ Oscillator Characteristics ■ Under Recommended Conditions	■ Actual Load / Power Supply ■ Thermal / Termination Conditions	■ Component Variations ■ Mounting Conditions ■ Actual Environment
NOT CONFIRMED **Performance on the Actual Board**	NOT CONFIRMED **Actual Layout and Surrounding Circuits**	NOT CONFIRMED **Production Variations and Long-Term Stability**	CONFIRMED **Performance and Design Margin**

Candidate Selection: Check Basic Specifications and Evaluation Conditions | **Adoption Decision: Confirm Performance in the Actual Environment**

Use data from each stage together; make the final adoption decision under actual system conditions.

Different Evaluation Conditions Can Change the Meaning of the Data

When comparing datasheet specifications, it is important not to judge performance based on numerical values alone. Phase noise and RMS phase jitter can vary depending on measurement conditions such as the oscillation frequency, integration bandwidth, termination conditions, and power-supply conditions. Data obtained under different conditions therefore cannot be directly compared. For example, changing the integration bandwidth will also change the RMS phase jitter value. In an actual system, factors such as the PCB transmission path may also alter the jitter characteristics observed at the measurement point.
In IEEE P802.3dj, measurement methods that take into account the effects of channel-induced jitter amplification are also under discussion. When evaluating clock performance, it is therefore important to confirm compatibility with the system's clock and data recovery (CDR) requirements and overall jitter budget, while also considering the intended operating conditions, including high-temperature environments, power-supply variations, and PCB transmission paths.

Standalone Oscillator Evaluation Data and System-Level Evaluation Data Serve Different Purposes

Standalone oscillator evaluation data and system-level evaluation data serve different purposes. Metrics such as phase noise, RMS phase jitter, temperature characteristics, and power-supply noise immunity provide insight into the performance of the oscillator itself and can be used to compare candidate products.
By contrast, evaluations such as eye diagrams and bit error rate (BER) measurements are used to assess the performance of the overall system, taking into account factors such as the PCB configuration, DSP, CDR settings, transmission path, and thermal environment. Even when an oscillator demonstrates excellent standalone characteristics, it may not necessarily deliver the expected results when integrated into the actual system.
When selecting candidate products, these two types of evaluation data should therefore be used as complementary sources of information. Ultimately, performance should be verified under the conditions of the actual system in which the oscillator will be used.

Standalone Clock Evaluation Results Alone Cannot Determine Compatibility with Your System

Standalone clock evaluation results alone are not sufficient to determine whether a clock is suitable for a specific system environment. Actual performance can be affected by numerous factors, including the PCB configuration, termination circuit, power and GND design, decoupling, and thermal effects from surrounding components.
Even if excellent phase noise and RMS phase jitter performance is achieved on an evaluation board, the same performance may not necessarily be reproduced on the actual system PCB. In 1.6T optical communication in particular, the effects of heat generated by high-density integration and crosstalk are also important factors that cannot be overlooked.
While standalone evaluation data is useful for selecting candidate products, planning evaluations under actual PCB, load, and temperature conditions can help reduce design risk and verify compatibility with the intended system environment.

Evaluation Results from Prototype PCBs Do Not Necessarily Guarantee Performance in Mass Production or Actual Operating Environments

Even if no issues are identified on a prototype PCB, the same results may not necessarily be achieved on mass-production boards or under actual operating conditions. In mass production, factors such as component tolerances, mounting conditions, power-supply quality, and temperature variations can introduce issues that were not apparent during the prototype stage.
If BER degradation or unstable synchronization is discovered during the later stages of development, it may lead to PCB redesign or revisions to the mass-production schedule. It is therefore important to define the required clock quality and evaluation conditions from the early stages of system design and select candidate devices with sufficient design margin.
Establishing an evaluation plan that takes mass production into account early in the development process can help minimize costly design rework later on.

Checklist for Selecting and Evaluating Clocks for 1.6T Optical Communication

When selecting a clock device, it is important not to make an adoption decision based solely on datasheet specifications, but to confirm that all the information required for the specific system design conditions is available. Rather than serving as a tool for simply ranking products, this checklist can be used as a practical resource for determining whether you are fully prepared to proceed with evaluation.

First, organize candidate products according to the three key evaluation criteria: phase noise / RMS phase jitter, frequency-temperature characteristics, and compatibility with specifications and operating conditions. Then, clearly define the evaluation objectives, evaluation environment, and acceptance criteria to determine whether the necessary preparations are in place for meaningful verification under your own system conditions.

Rather than treating the acquisition of samples as the objective itself, designers should first establish what needs to be evaluated and under what conditions. Taking this approach before beginning evaluation can help minimize costly design rework during the later stages of development.

Checklist

＜Phase Noise / RMS Phase Jitter＞

- ☐ Have you checked the phase noise?
- ☐ Have you reviewed the entire phase noise plot?
- ☐ Have you checked the RMS phase jitter?
- ☐ Have you confirmed the frequency conditions used for the phase noise measurements?
- ☐ Have you confirmed the integration bandwidth?
- ☐ Have you confirmed other measurement conditions, such as supply voltage and load conditions?

＜Frequency-Temperature Characteristics＞

- ☐ Have you checked the frequency-temperature characteristics?
- ☐ Does the device support the intended operating temperature range?
- ☐ Have you confirmed the evaluation method under high-temperature and actual load conditions?

＜Compatibility with Specifications and Operating Conditions＞

- ☐ Does the device support the required operating frequency?
- ☐ Does it support the required output format?
- ☐ Have you confirmed the recommended termination conditions?
- ☐ Is the supply voltage compatible with your circuit requirements?
- ☐ Have you confirmed the recommended power, GND, and decoupling conditions?
- ☐ Have you identified the characteristics that need to be evaluated under the expected operating conditions, such as power supply variations, vibration, and acceleration?
- ☐ Is the package size compatible with your design?
- ☐ Are the recommended land pattern and mounting conditions compatible with your design?

＜Evaluation Objectives and Environment＞

- ☐ Is the evaluation objective clearly defined?
- ☐ Are the parameters to be verified during evaluation clearly defined?
- ☐ Can you provide the required evaluation environment?
- ☐ Do you have access to the necessary measurement equipment?
- ☐ Are the evaluation conditions clearly defined?
- ☐ Are the acceptance criteria for the evaluation results clearly defined?

The objective is not necessarily to satisfy every item on this list. Instead, use the checklist to ensure that no evaluation criteria required for your specific system design conditions have been overlooked.

KCRO-05 as a Candidate Clock for 1.6T Applications

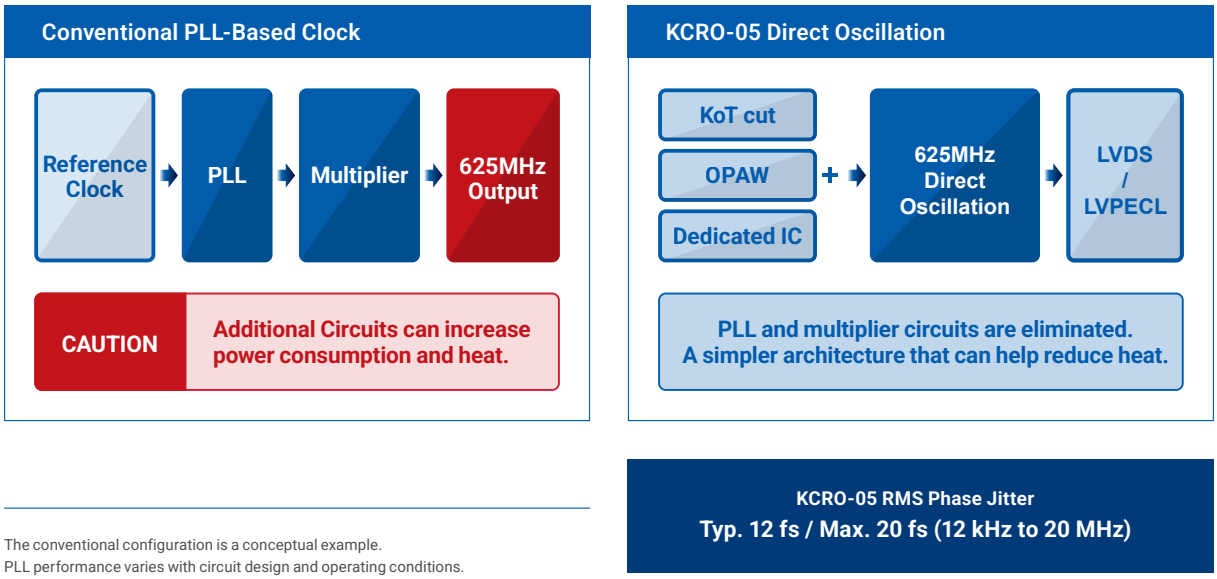
Based on the evaluation criteria outlined above, clocks for 1.6T optical communication require more than just low phase jitter. Their overall suitability must also be evaluated in terms of factors such as temperature characteristics and mounting conditions. The KCRO-05 is one clock that can be considered based on these evaluation criteria.
This section introduces the design concept and key technical features of the KCRO-05, along with the specifications that should be considered during evaluation.

Direct 625 MHz Fundamental-Mode Oscillation Without a PLL

For clocks used in 1.6T optical communication, it is important to minimize phase noise and jitter at the clock source itself. The KCRO-05 employs a design that generates 625 MHz directly in the fundamental mode, without using a PLL or frequency multiplier circuit.
Depending on their configuration and design conditions, conventional PLLs and frequency multiplier circuits can introduce phase noise and spurious components (spurs). A design that generates the required signal directly at the clock source without additional signal processing is therefore one effective approach to minimizing potential sources of jitter.

Comparison of 625 MHz Clock Generation Architectures

Conventional PLL-based clock generation and KCRO-05 direct oscillation.



KCRO-05 RMS Phase Jitter
Typ. 12 fs / Max. 20 fs (12 kHz to 20 MHz)

The conventional configuration is a conceptual example.
PLL performance varies with circuit design and operating conditions.

The PLL-less direct oscillation architecture of the KCRO-05 is designed to suppress jitter sources associated with PLLs and frequency multiplier circuits at the clock-generation stage. IEEE P802.3dj has also discussed jitter evaluation using metrics such as JHrms and J4u. From the perspective of ensuring the clock quality required for these next-generation high-speed interfaces, a PLL-less architecture represents one effective design approach.
For the KCRO-05, the crystal resonator and dedicated IC were developed together, enabling impedance matching and drive conditions to be optimized in pursuit of low phase jitter performance. Technical materials submitted to the IEEE P802.3dj Task Force have also indicated that jitter in transmitted signals can affect bit error rate (BER) and FEC performance.
When evaluating the KCRO-05, designers should therefore consider its design philosophy of minimizing jitter originating at the clock source and verify that its performance is consistent with the overall system jitter budget of their specific application.

KoT Cut and OPAW Technologies for Ultra-Low Phase Jitter

The low phase jitter performance of the KCRO-05 is supported by a design approach that optimizes the crystal resonator and oscillator circuit as an integrated system. By combining River Eletec's proprietary KoT cut® crystal-cut technology with OPAW® (Orthogonal Plate Acoustic Wave) technology, the KCRO-05 achieves direct 625 MHz fundamental-mode oscillation.
River Eletec also developed a dedicated IC specifically optimized for KoT cut®, enabling impedance matching and drive level to be optimized for the crystal resonator. This results in RMS phase jitter of Typ. 12 fs and Max. 20 fs over an integration bandwidth of 12 kHz to 20 MHz.
When evaluating the KCRO-05, it is important to consider not only its phase noise / RMS phase jitter, but also its frequency-temperature characteristics and compatibility with the actual mounting conditions of the target system.

KCRO-05 Qualification Test Results for Harsh Operating Environments

For 1.6T optical communication equipment, it is important to verify clock reliability under demanding operating environments, taking into account factors such as the heat generated by high-density integration. The KCRO-05 has undergone a series of qualification tests under specified conditions to verify product reliability under harsh environmental stresses, including extreme temperatures and vibration.
The qualification testing included multiple tests designed to simulate high-temperature conditions, temperature variations, vibration, and other environmental stresses. The KCRO-05 met the specified acceptance criteria for each test. These results provide objective product data for assessing the reliability and robustness of the KCRO-05 and can serve as one of the factors considered when evaluating candidate clock devices.

KCRO-05 Qualification Test Results

Test Item	Test Conditions	Result
Low-Temperature Storage	1,000 hours at -55 ±5°C	Pass
Resistance to Soldering Heat	Pb-free profile (260°C)	Pass
High-Temperature Storage Life	1,000 hours at 125°C	Pass
Temperature and Humidity	1,000 hours at 85°C / 85% RH	Pass
Temperature Cycling	1,000 cycles from -55°C to 125°C	Pass
Mechanical Shock	1,500g peak, 0.5 ms pulse, 5 pulses in each of 6 directions	Pass
Variable-Frequency Vibration	20g peak, 20–2,000 Hz, X, Y & Z axes	Pass
High-Temperature Operating Life	1,000 hours at 125°C, Vmax	Pass
ESD (HBM)	2,000 V (tested at room temperature / hot / cold)	Pass

Key KCRO-05 Specifications to Check Before Evaluation

To conduct an efficient evaluation, it is important to compare the key specifications of the KCRO-05 against your system requirements in advance. Key parameters to confirm include the oscillation frequency, RMS phase jitter, output format, supply voltage, operating temperature range, and package size.
For RMS phase jitter, designers should confirm not only the numerical value but also the associated measurement conditions, such as the 12 kHz to 20 MHz integration bandwidth. Reviewing the phase noise plot can also provide insight into noise characteristics at different offset frequencies that may not be apparent from the integrated jitter value alone.
Specifications should not be viewed simply as a means of determining whether one product is superior to another. Instead, they should be used to assess whether the device is compatible with the specific circuit conditions and design requirements of the target system.

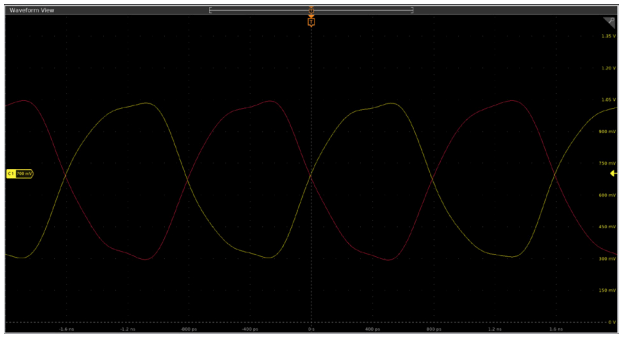
KCRO-05 Specification

Parameter	Specification
Oscillation Frequency	625 MHz
RMS Phase Jitter	Typ. 12 fs / Max. 20 fs (12 kHz–20 MHz)
Output Format	LVDS / LVPECL
Supply Voltage	LVDS: 1.8 V / 2.5 V / 3.3 V; LVPECL: 2.5 V / 3.3 V
Operating Temperature Range	-40°C to +105°C
Package Size	2.5 × 2.0 × 0.85 mm Max.

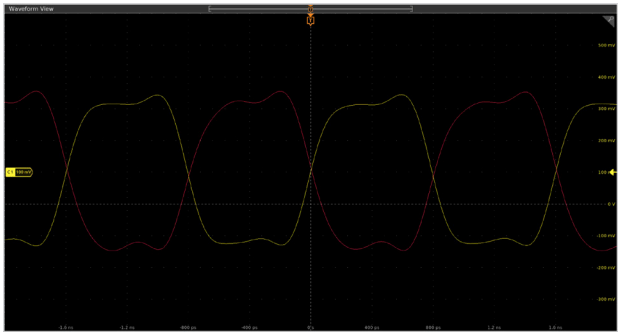
When evaluating the KCRO-05, it is important to check not only specifications such as the output format but also the actual output waveforms. The figure below shows the LVPECL and LVDS output waveforms at 625 MHz and 3.3 V. Reviewing the waveform for each output format can help assess compatibility with your circuit conditions.

Waveform

625MHz / LVPECL / 3.3V

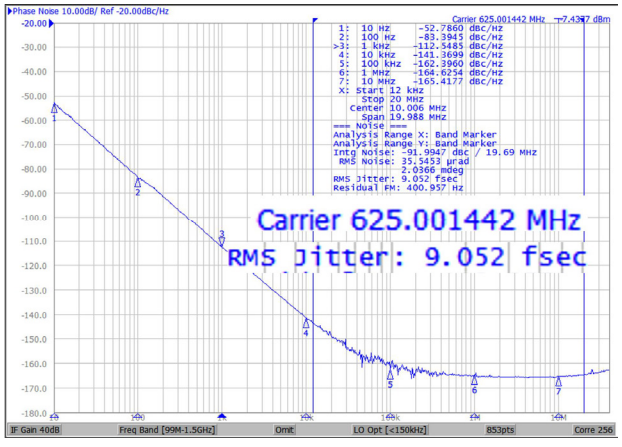


625MHz / LVDS / 3.3V

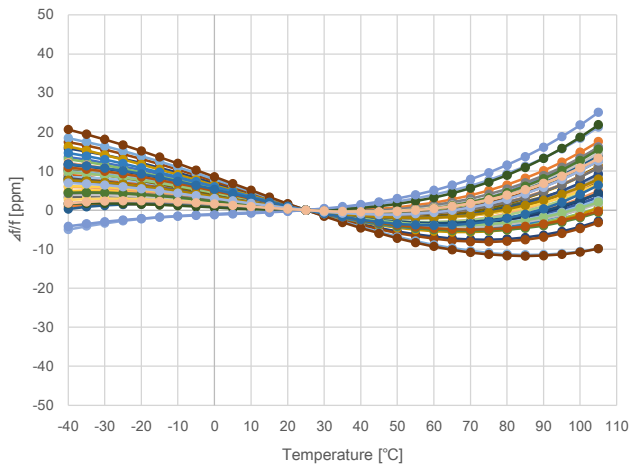


When evaluating the KCRO-05, it is useful to examine not only the integrated RMS phase jitter value, but also the phase noise characteristics at different offset frequencies and the trend in frequency variation across the intended operating temperature range. This makes it easier to assess compatibility with the actual operating conditions of the target system.
The figures below provide examples of the KCRO-05's phase noise / RMS phase jitter characteristics and frequency-temperature characteristics.

PHASE NOISE, PHASE JITTER



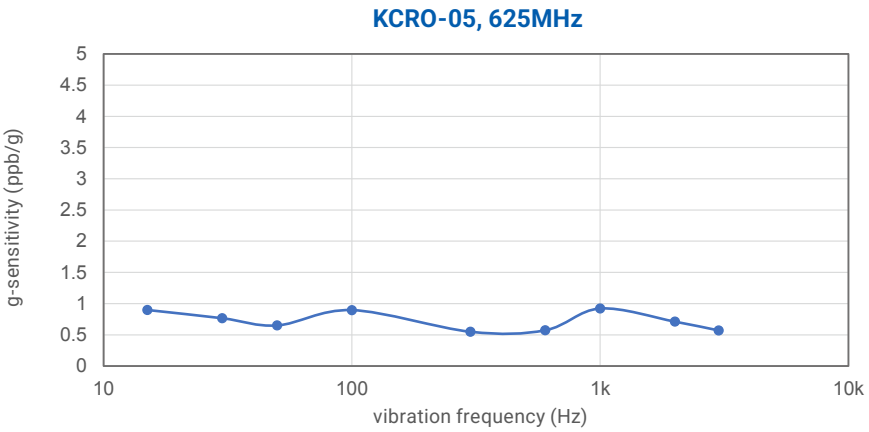
FREQUENCY vs. TEMPERATURE CHARACTERISTICS



Source: RIVER ELETEC CORPORATION, "KoT cut OPAW Crystal Oscillator KCRO-05 Preliminary"

In operating environments where vibration or acceleration may affect performance, g-sensitivity (acceleration sensitivity) is another important characteristic to evaluate. G-sensitivity indicates the effect of acceleration on the oscillation frequency and can provide useful information when assessing clock stability under the expected operating conditions.

g-sensitivity



Source: RIVER ELETEC CORPORATION, "KoT cut OPAW Crystal Oscillator KCRO-05 Preliminary"

FAQ: What to Check Before Evaluating the KCRO-05

When evaluating the KCRO-05, designers may have questions such as how jitter values should be compared and whether datasheet specifications alone are sufficient for making a selection decision.
Based on the evaluation criteria discussed above, this section addresses some of the most common questions that may arise when considering the KCRO-05 for a specific application.

Q Is lower clock jitter always better?

A. Jitter performance cannot be evaluated based on the jitter value alone.

RMS phase jitter is calculated by integrating phase noise over a specified frequency range. Therefore, the resulting value will vary depending on the integration bandwidth and measurement conditions. For a meaningful comparison, the data must be measured under the same conditions, including the oscillation frequency, integration bandwidth (e.g., 12 kHz to 20 MHz), and phase-noise measurement conditions.
Rather than simply comparing numerical jitter values, it is important to assess whether the clock provides the required performance for your system, taking into account factors such as the system's timing margin and jitter budget.

Q Can I determine whether to use the KCRO-05 based on catalog specifications alone?

A. We do not recommend making a final selection based solely on catalog specifications.

Catalog specifications are useful for identifying potential candidates, but actual performance can also be affected by factors such as the PCB configuration, termination conditions, power supply and ground design, decoupling, and thermal interaction with surrounding components.
Catalog data should therefore be used to narrow down potential candidates, while final suitability should be verified through testing under conditions representative of the actual application, including the target PCB, load conditions, and operating temperature.

Q If there are no issues with the prototype board, can we expect the same performance in mass production?

A. Performance in mass production cannot be guaranteed based solely on evaluation results from a prototype board.

In 1.6T optical communication systems, multiple factors—including power supply noise, PCB layout, the thermal environment, and interference from surrounding circuitry—can interact, potentially causing issues that were not apparent during prototyping to emerge in mass production.
Defining requirements for jitter, frequency accuracy, temperature characteristics, and other key parameters from the early stages of design, and conducting evaluations with sufficient design margin, can help minimize the need for costly redesigns later in the development process.

Q What should I evaluate when considering the KCRO-05?

A. It is important to assess suitability for your application based on three key evaluation criteria.

The three key areas to evaluate are phase noise/RMS phase jitter, frequency stability over temperature, and compliance with the required specifications and operating conditions. The KCRO-05 qualification test results can also provide useful information for assessing the product's reliability and robustness under demanding environmental conditions.
Compare factors such as the oscillation frequency, integration bandwidth, output format, termination conditions, and operating temperature range against your system requirements to determine the KCRO-05's overall suitability for your application.

Q What should I prepare before evaluating the KCRO-05?

A. Clearly define your evaluation objectives and system requirements in advance.

In addition to the required frequency, output format, expected operating temperature, and PCB configuration, it is important to identify the parameters you want to evaluate and the evaluation environment.
If you require additional information, such as phase-noise data or temperature-characteristics graphs, consulting River Eletec about recommended circuit configurations and measurement conditions before arranging an evaluation board or samples can help ensure a smoother and more effective evaluation process.

[Summary]
Start by Discussing Your Evaluation Conditions

When selecting a clock for 1.6T optical communication systems, it is important to consider not only numerical specifications such as phase noise and RMS phase jitter, but also temperature characteristics, mounting conditions, and compatibility with your PCB and operating environment. Catalog specifications and KCRO-05 qualification test results can help narrow down potential candidates, but final suitability should be verified in your own system environment.

When considering an evaluation of the KCRO-05, defining your requirements in advance—including the operating frequency, output format, temperature conditions, PCB configuration, and parameters to be evaluated—will make it easier to determine the appropriate evaluation approach. If you are unsure about the evaluation conditions or measurement methods, please contact us before beginning sample evaluation.

[For Those Considering Evaluating the KCRO-05]

If you are considering evaluating the KCRO-05, please contact River Eletec for guidance on evaluation methods and suitability for your design. Technical information, including recommended circuit configurations, termination conditions, and measurement setups, is available to help you determine the appropriate evaluation approach for your specific application.

[Discuss KCRO-05 Evaluation Methods and Implementation Requirements]

References

Adee Ran, Proposed Tx Jitter Methodology and Limit Values (Comments #204, #236 Against D1.0), IEEE P802.3dj Task Force, May 2024.
River Eletec Corporation, KoT-Cut OPAW Crystal Oscillator KCRO-05 Product Datasheet (Preliminary), April 21, 2026.
River Eletec Corporation, Development and Mass Production Plan for the KCRO-05, a Strategic New Product for AI Data Centers, December 11, 2025.

Notes

*1 The IEEE P802.3dj Task Force document cited in this material is not an IEEE standard itself, but rather a technical contribution submitted and discussed as part of the standardization process. Jitter metrics such as J3u and J6u are also being considered as part of the standardization process for 200G/lane electrical interfaces and have not been finalized as part of the IEEE 802.3dj standard.

*2 The transmit-signal jitter metrics discussed in this material (such as JRMS) and the RMS phase jitter of a clock oscillator cannot be directly compared numerically because they differ in terms of the signal being measured, measurement methodology, and integration bandwidth.

*3 The KCRO-05 qualification test results presented in this material are the results of reliability testing conducted on the crystal oscillator itself under specified conditions. When the device is implemented in an actual system, factors such as PCB transmission paths and power supply noise must also be taken into account, and compatibility with the overall system jitter budget must be verified. The qualification test results should be used as a reference for assessing the reliability of the product itself, while final suitability should be determined through evaluation in the intended system environment.

*4 The KCRO-05 specifications presented in this material are representative values based on the product specifications. When considering adoption of the KCRO-05, please refer to the latest datasheet and technical documentation.

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